COMPUTER SYSTEM EMBEDDING SEQUENTIAL BUFFERS THEREIN FOR IMPROVING THE PERFORMANCE OF A DIGITAL SIGNAL PROCESSING DATA ACCESS OPERATION AND A METHOD THEREOF

ABSTRACT OF THE DISCLOSURE

Provided is a computer system embedding buffers therein for improving the performance of a digital signal processing (DSP) data access operation and a method thereof. The computer system comprises a DSP core, a data cache, first and second buffer modules, and an external memory. The computer system further comprises a central processing unit (CPU) core. The CPU core executes instructions to control operations in the system and the DSP core processes data in accordance with instructions provided from the CPU core. The data cache stores temporary data generated during operations in the DSP core. The first buffer module stores input data forwarded to the DSP core while the second buffer module stores output data provided from the DSP core. The external memory stores the temporary data, the input data, and the output data. The computer system accesses input and output data of the DSP core by way of the first and second buffer modules and uses separated storage fields for the input data, the temporary data, and the output data, in the external memory, which prevent degradation of the performance of the data cache and DSP functions.